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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,470	03/29/2001	Yoshihiro Yoneda	82-01	5656

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EXAMINER
PATEL, ISHWARBHAI B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/820,470	YONEDA, YOSHIHIRO
	Examiner	Art Unit
	Ishwar (I. B.) Patel	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) *5,6,25-39 and 47-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7-24 and 40-46* is/are rejected.

7)☒ Claim(s) *53-54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *30 July 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on July 30, 2002. These drawings are approved.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7-10, 12, 15, 42, 44, 46, 53 and 54 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 7 and 8, it is not clear whether the terminals are covered or the wiring lines are covered. Only terminals are there on the outermost layers. Wiring lines are already covered by the insulating layers.

Regarding claim 9, it is not clear how spacing between two terminals will be 200 micrometer or more with a pitch of 100 micrometer of less.

Regarding claims 10 and 42, it is not clear what is meant by "the conductive members in an area, over which the part is mounted, of the outermost layer of wiring lines connected with the connection terminals are arranged at a uniform density as a

whole", and in particular, what is meant by "as a whole". There will be pads and traces on the top layer with different width and is not clear what kind of uniformity is there on the top layer. Further, what is "conductive members?" Does it include terminals, via connections and traces?

Regarding claims 12 and 44, it is not clear what is meant by "conductive members in the area, over which the part is mounted, of each of the layers of wiring lines located below the outermost layer of wiring lines connected with the connecting terminals are arranged at a uniform density as a whole". Is it the spacing between the wiring identical on all layers or the shape / width of wiring is identical on all the layers? Does the conductive member includes the via holes?

Regarding claims 15 and 46, it is not clear what is meant by "the conductive member at each of the layers of wiring lines below the outermost layer of wiring lines are arranged at substantially the same density as the density of the conductive members at the outermost wiring lines". Is it the identical wiring on all the layers or same material density on all the layers?

Regarding claims 53 and 54, it is not clear what is meant by "so as to be each located under a respective connecting terminal". Does it mean that the density is same and also the wiring lines are located under a respective connecting terminal? Examiner understood the number of connecting terminals and number of wiring lines are same

and the wiring lines are located under respective terminal on each layer below that of the connecting terminals.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1,4,7 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Arima et al., US Patent No. 5,375,042, hereafter Arima.

Regarding claims 1, Arima, submitted with first action, discloses a surface-mounting substrate for mounting a part thereon, which comprises a core substrate, a plurality of layers of patterned wiring lines, which are separated from each other by an insulation layer interposed there between, vias piercing through the insulation layer to connect the wiring lines at the adjacent layers to each other (thin film circuit 2 with X layer wiring, Y layer wiring and via holes, see figure 1, column 5, line 1-20),

and a layer of connecting terminals to mount a part on the surface-mounting substrate, each of the connecting terminals connecting with the wiring line at the outermost layer of wiring lines, wherein the connecting terminal is filled in an outermost insulation layer provided at the surface of the surface-mounting substrate, and has a surface exposed at substantially the same level as the level of the surface of the outermost insulation layer, the connecting terminal being provided on its surface with

solder material (connecting pad 5 in the surface connecting layer 19, with solder on both pad 5 of the circuit board and pad 7 of the semiconductor chip, see figure 1, column 5, line 1-20, and 35-40).

Regarding claim 40, Arima discloses all the features of the claimed invention including the bump on the part, (pad 7 on semiconductor chip with solder, column 5, line 35-40).

Regarding claims 4, Arima further discloses semiconductor device (semiconductor chip 6,see figure 1).

Regarding claim 7, Arima further discloses the wiring lines covered with a cover material, (insulation layer 14 and surface layer 19, see figure 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8-15, 18-24 and 42-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arima et al., US Patent No. 5,375,042, as applied to claim 1 above.

Regarding claim 8, though Arima does not explicitly disclose a solder resist layer, use of such layer on topmost surface is known in the art for protecting the outer surface form environment and also to avoid short-circuiting between adjacent pads. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Arima with top most layer made of solder resist material, in order to protect the surface from environmental effect and any damage during assembly and to avoid short circuit. Further, it has been held to be within general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125, USPQ 416.

Regarding claim 9, Arima does not explicitly disclose a terminal pitch of 100 micrometer or less, the crux of thin film wiring is to increase the pad density for flip chip installation of the chip to reduce the distance between the chip and the terminal, and pitch as low as 80 micrometer is known in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Arima with the terminal pitch of 100 micrometer or less.

Regarding claims 10, 12, 15, 42, 44 and 46, the applicant is claiming the arrangement of the terminal, the wiring lines on top surface and below the top surface and their uniform distribution. Though Arima does not explicitly disclose the uniform density of the terminal and internal wiring pattern, the terminals on the top surface will depend upon the number of electrodes on semiconductor device to be connected and

the arrangement and routing of the wiring pattern will be arranged to get maximum possible component density of the component mounting pad without compromising the quality of the board, such as withstanding the thermal expansion contraction without warping or crack, better heat dissipation rate, rigidity, avoiding short circuiting etc. Nevertheless, based on the severity of the system, the metal density on various layers will be adjusted to have better performance. Therefore, it would have been obvious to one having ordinary skill in the art the time the invention was made to provide the circuit board of Arima with terminal arrangement and wiring arrangement uniformly distributed in order to get higher component density without compromising the quality and improving the reliability and avoid uneven expansion / contraction.

Regarding claim 11,13, 43 and 45, Arima further discloses the conductive member including the terminals and wiring lines and via, see figure 1.

Regarding claim 14 and 18, though Arima does not explicitly discloses a power or ground layer, it is inherent to use a layer as power layer for distributing the power or a ground layer for providing grounding or shielding in the circuit assembly and further meshed power / ground layers are known in the art and is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art the time the invention was made to provide the circuit board of Arima with a power layer and/or ground layer in order to distributing the power required or to provide grounding or shielding for safety.

Regarding claims 19-24, the applicant is claiming various width and spacing of terminals, wiring and the via. Though, Arima does not explicitly disclose such width and spacing of the terminals, wiring and via, with thin film manufacturing, it is inherent to have high density with small size features and it is known in the art to have such features for getting high density of component accommodated in a package. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the circuit board of Arima with the via dimensions as claimed in claims 19-24 in order to have circuit structure with high component mounting capacity.

8. Claims 16, 17 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arima et al., US Patent No. 5,375,042 as applied to claim 1 above, and further in view of Hsu et al., US Patent No. 6,242,815, hereafter Hsu, submitted with first action.

Regarding claims 16,17 and 41, though Arima does not disclose the dummy member, such dummy member such as, dummy pad or dummy wiring is known in the art either for controlling the thermal coefficient of the board or increasing strength or rigidity of the board. Further providing dummy member is quite often used for a universal circuit board for future changes or repair. Hsu discloses dummy pads for increasing the rigidity and the strength of the mount area. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

provide the circuit board of Arima with dummy member as taught by Hsu to maintain the rigidity and strength and the resultant reliable and long service life. Further, regarding claim 41, Arima does discloses the semiconductor chip, see figure 1.

Response to Arguments

9. Applicant's arguments with respect to claims 1 and 40 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the obviousness rejection of power / ground layers, it is well known to one of ordinary skilled in the art to provide power / ground layer in the circuit board depending upon the requirement.

Regarding various features of the conductive element such as, width, diameter, pitch and distribution thereof, it is the crux of the invention of the thin film circuit boards to have the smaller sizes to increase the component density without compromising the quality. Further, the examiner recognize that references can not be arbitrarily combined and there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken, as a whole would suggest to one of ordinary skill in the art.

Allowable Subject Matter

10. Claims 53 and 54 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ito discloses the thickness of thick film about 100 micrometer and that of thin film about 20 to 30 micrometer.

Andou et al, discloses wiring width of about 30 micrometers and hole diameter about 30 micrometers.

Iijima et al, submitted with first action, discloses terminals exposed on the same level as that of the topmost insulation layer.

Tanaka discloses solder bump on the substrate pad.

Goodman et al., Hirano and Schaper discloses power / ground layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (703) 305 2617. The examiner can normally be reached on M-F (6:30 - 4) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L Talbott can be reached on (703) 305 9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305 3431 for regular communications and (703) 305 7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

ibp
November 22, 2002

ALBERT W. PALADINI
PRIMARY EXAMINER